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EXAMINER	
ROSSOSHEK, YELENA	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/040,055	FALBO ET AL.	
	Examiner	Art Unit	
	Helen Rossoshek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11,33,37-43 and 55-99* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11,33,37-43 and 55-99* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the Application 10/040,055 filed 12/31/2001 and amendment filed 11/30/2004.

2. Claims 11, 33, 37-43, 55-99 remain pending in the Application. Claims 55-99 have been added to the Application.

3. Applicant's amendment has been fully considered. Examiner does not find them persuasive.

Specification

4. The disclosure is objected to because of the following informalities: Page 23 Paragraph [0076]: the word "beatification" needs to be replaced by --beautification--.

Appropriate correction is required.

Claim Objections

5. Claim 87 is objected to because of the following informalities: using an indefinite language ("can").

Appropriate correction is required.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 11, 33, 37-43 and 55-99 are rejected under 35 U.S.C. 102(e) as being anticipated by Agrawal et al. (US Patent 6,523,162).

8. The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

With respect to claims 11 Agrawal et al. teaches a method for performing a layout beautification operation on an integrated circuit (IC) layout comprising a plurality of polygons (layout features in the first portion) using the **shape-based approach** which enables accurate and efficient application of **layout modifications** (col. 14, ll.16-19; col. 5, ll.51-52; col. 8, ll.45-48), the method comprising applying a first action to a first portion of the IC layout responsive to determining that a first shape associated with the first action matches the first portion of the IC layout by applying the first action to the first set of layout features (col. 14, l.31) matching with the **first shape** and the second portion **of the first plurality of properties** (col. 14, ll.24-30), the first shape comprising at least a first edge and a second edge related according to a defined property, the first shape being configured to match a first type of layout imperfection wherein the layout features comprises the polygon or groupings of polygons representing the layout imperfection (col.14, ll.20-23); the second edge being contiguous with and substantially perpendicular to the first edge as shown on the Figs. 4a, 4b and 4c which provide

examples of basic shapes wherein the second edge E412 is contiguous and substantially perpendicular to the first edge E411 (col. 6, ll. 35-37); and wherein the first shape further comprises: a third edge, the third edge being contiguous with and substantially perpendicular to the second edge as shown o the Figs. 4a-4c, 5a-5d, 6a-6e, 7a-7c and particularly according the Fig. 4b wherein the third edge E423 is contiguous and substantially perpendicular with the second edge E422; a fourth edge, the fourth edge being contiguous with and substantially perpendicular to the third edge as shown o the Figs. 4a-4c, 5a-5d, 6a-6e, 7a-7c and particularly according the Fig. 4c wherein the fourth edge E434 is contiguous and substantially perpendicular with the third edge E433; and a fifth edge, the fifth edge being contiguous with and substantially perpendicular to the fourth edge as shown o the Figs. 4a-4c, 5a-5d, 6a-6e, 7a-7c and particularly according the Fig. 4c wherein the fifth edge E435 is contiguous and substantially perpendicular with the fourth edge E434 (col. 6, ll.44-51; col. 17, ll.10-21), wherein none of the first edge, the second edge, the third edge, the fourth edge, and the fifth edge are substantially side- by-side with each other as shown on the Fig. 4c.

With respect to claim 33 Agrawal et al. teaches a software program for performing layout beautification on a plurality of polygons in an integrated circuit (IC) layout, each of the plurality of polygons comprising a plurality of features, the software program (col. 19, ll.25-26; col. 20, ll.1-2) comprising: a first set of instructions for comparing a first shape to the plurality of features in each of the plurality of polygons to identify a first set of matching layout features, the first shape comprising at least a first edge and a second edge related according to a first property within the software

wherein any programming code having plurality of sets of code has an ability of any sequence of having the instructions in the whole code (col. 20, ll.3-7; ll.20-23); a second set of instructions for performing a first layout beautificati6n action on each of the first set of matching layout features within the code processing a first action (first layout beautification action) within the software wherein any programming code having plurality of sets of code has an ability of any sequence of having the instructions in the whole code (col. 20, ll.24-25); third set of instructions for defining the first shape according to a set of user inputs within the software wherein any programming code having plurality of sets of code has an ability of any sequence of having the instructions in the whole code (abstract; col. 20, ll.20-22); within the ability of the system and software (programming code) for providing shapes/action as retrieving from a remote source or defining by the user (abstract).

With respect to claim 37 Agrawal et al. teaches a software program for performing layout beautification on a plurality of polygons in an integrated circuit (IC) layout, each of the plurality of polygons comprising a plurality of features, the software program (col. 19, ll.25-26; col. 20, ll.1-2) comprising: a first set of instructions for comparing a first shape to the plurality of features in each of the plurality of polygons to identify a first set of matching layout features, the first shape comprising at least a first edge and a second edge related according to a first property within the software wherein any programming code having plurality of sets of code has an ability of any sequence of having the instructions in the whole code (col. 20, ll.3-7); a second set of instructions for performing a first layout beautificati6n action on each of the first set of

matching layout features within the code processing a first action (first layout beautification action) within the software wherein any programming code having plurality of sets of code has an ability of any sequence of having the instructions in the whole code (col. 20, ll.16-19); third set of instructions for defining the first shape according to a set of user inputs within the software wherein any programming code having plurality of sets of code has an ability of any sequence of having the instructions in the whole code (abstract; col. 20, ll.20-22); a third set of instructions for loading the first shape from across a network within the code processing a first action (first layout beautification action) within the software wherein any programming code having plurality of sets of code has an ability of any sequence of having the instructions in the whole code (col. 13, ll.51-53; col. 20, ll.23-24).

With respect to claim 38 Agrawal et al. teaches a software program for performing layout beautification on a plurality of polygons in an integrated circuit (IC) layout, each of the plurality of polygons comprising a plurality of features, the software program (col. 19, ll.25-26; col. 20, ll.1-2) comprising: a first set of instructions for comparing a first shape to the plurality of features in each of the plurality of polygons to identify a first set of matching layout features, the first shape comprising at least a first edge and a second edge related according to a first property within the software wherein any programming code having plurality of sets of code has an ability of any sequence of having the instructions in the whole code (col. 20, ll.3-7); a second set of instructions for performing a first layout beautificati6n action on each of the first set of matching layout features within the code processing a first action (first layout

beautification action) within the software wherein any programming code having plurality of sets of code has an ability of any sequence of having the instructions in the whole code (col. 20, ll.16-19); third set of instructions for defining the first shape according to a set of user inputs within the software wherein any programming code having plurality of sets of code has an ability of any sequence of having the instructions in the whole code (abstract; col. 20, ll.20-22); a third set of instructions for defining the first layout beautification action according to a set of user inputs within the ability of the system and software (programming code) for providing shapes/action as retrieving from a remote source or defining by the user (abstract).

With respect to claim 39 Agrawal et al. teaches a software program for performing layout beautification on a plurality of polygons in an integrated circuit (IC) layout, each of the plurality of polygons comprising a plurality of features, the software program (col. 19, ll.25-26; col. 20, ll.1-2) comprising: a first set of instructions for comparing a first shape to the plurality of features in each of the plurality of polygons to identify a first set of matching layout features, the first shape comprising at least a first edge and a second edge related according to a first property within the software wherein any programming code having plurality of sets of code has an ability of any sequence of having the instructions in the whole code (col. 20, ll.3-7); a second set of instructions for performing a first layout beautificati6n action on each of the first set of matching layout features within the code processing a first action (first layout beautification action) within the software wherein any programming code having plurality of sets of code has an ability of any sequence of having the instructions in the whole

code (col. 20, ll.16-19); third set of instructions for defining the first shape according to a set of user inputs within the software wherein any programming code having plurality of sets of code has an ability of any sequence of having the instructions in the whole code (abstract; col. 20, ll.20-22); a third set of instructions for loading the first shape from across a network within the code processing a first action (first layout beautification action) within the software wherein any programming code having plurality of sets of code has an ability of any sequence of having the instructions in the whole code and within the ability of the system and software (programming code) for providing shapes/action as retrieving from a remote source or defining by the user (abstract; col. 13, ll.51-53; col. 20, ll.23-24).

With respect to claim 40 Agrawal et al. teaches a software program for performing layout beautification on a plurality of polygons in an integrated circuit (IC) layout, each of the plurality of polygons comprising a plurality of features, the software program (col. 19, ll.25-26; col. 20, ll.1-2) comprising: a first set of instructions for comparing a first shape to the plurality of features in each of the plurality of polygons to identify a first set of matching layout features, the first shape comprising at least a first edge and a second edge related according to a first property within the software wherein any programming code having plurality of sets of code has an ability of any sequence of having the instructions in the whole code (col. 20, ll.3-7); a second set of instructions for performing a first layout beautification action on each of the first set of matching layout features within the code processing a first action (first layout beautification action) within the software wherein any programming code having plurality

of sets of code has an ability of any sequence of having the instructions in the whole code (col. 20, ll.16-19); a third set of instructions for comparing a second shape to the plurality of features in each of the plurality of polygons to identify a second set of matching layout features, the second shape comprising at least a third edge and a fourth edge related according to a second property within the software wherein any programming code having plurality of sets of code has an ability of any sequence of having the instructions in the whole code and within the ability of the system and software (programming code) for providing shapes/action as retrieving from a remote source or defining by the user (abstract; col. 19, ll.13-19); a fourth set of instructions for performing a second layout beautification action on the second set of matching layout features within the software wherein any programming code having plurality of sets of code has an ability of any sequence of having the instructions in the whole code (col. 19, ll.20-24).

With respect to claims 41-43 Agrawal et al. teaches:

claim 41: the first set of instructions and the second set of instructions are completely executed before the third set of instructions and the fourth set of instructions according the software wherein any programming code having plurality of sets of code has an ability of any sequence of having the instructions in the whole code and flexibility of executing sets of instructions in any sequence according the programming code via user inputs (col. 20, ll.16-19);

claim 42: the first set of instructions and the second set of instructions are executed concurrently, and wherein comparing the first shape to a selected one of the plurality of

features in each of the plurality of polygons is performed before comparing the second shape to the selected one of the plurality of features in each of the plurality of polygons according the software wherein any programming code having plurality of sets of code has an ability of any sequence of having the instructions in the whole code and flexibility of executing sets of instructions in any sequence according the programming code via user inputs (col. 3, ll.14-16; col. 19, ll.22-24);

claim 43: first action and the second action are incorporated in a lookup table (col. 2, ll.61-63; ll.65-67; Table 4).

With respect to claims 55 Agrawal et al. teaches a method for performing a layout beautification operation on an integrated circuit (IC) layout comprising a plurality of polygons (layout features in the first portion) using the **shape-based approach** which enables accurate and efficient application of **layout modifications** (col. 14, ll.16-19; col. 5, ll.51-52; col. 8, ll.45-48), the method comprising applying a first action to a first portion of the IC layout responsive to determining that a first shape associated with the first action matches the first portion of the IC layout by applying the first action to the first set of layout features (col. 14, l.31) matching with the **first shape** and the second portion **of the first plurality of properties** (col. 14, ll.24-30), the first shape comprising at least a first edge and a second edge related according to a defined property, the first shape being configured to match a first type of layout imperfection wherein the layout features comprises the polygon or groupings of polygons representing the layout imperfection (col.14, ll.20-23);

With respect to claims 56-64 Agrawal et al. teaches:

claim 56: the first action comprises adjusting the first type of layout imperfection by a fixed amount as shown on the Fig. 9b wherein a shape S_2 and a modified feature F_2 that could result from application of an action B (beatification process) associated with shape S_2, wherein action narrows and lengthens finger structures matching shape S_2 by a particular amount (col. 10, ll.64-67);

claim 57: the first type of layout imperfection covers a plurality of actual layout imperfections, each of the plurality of actual layout imperfections having a different set of actual properties, wherein the first action comprises making an adjustment according to the set of actual properties for each of the plurality of actual layout imperfections within plurality of shapes wherein each shape having set of properties and layout processing actions are based on the properties (col. 3, ll.24-26; col. 6, ll.14-18);

claim 58: the first action comprises replacing the first type of layout imperfection with a second shape within the catalog of shapes specifying actions as functions of the property variables of the shapes (col. 8, ll.37-39; col. 10, ll.34-36);

claim 59: the first edge and the second edge are not contiguous (col. 14, ll.43-45);

claim 60: the IC layout comprises a first layer and a second layer, the first edge being associated with the first layer, and the second edge being associated with the second layer (col. 7, ll.26-27);

claim 61: the first layer comprises a gate layer and the second layer comprises a wire layer as shown on the Fig. 6b wherein features 610, 620, 630 are depicted and feature 610 is used to form a gate (col. 7, ll.38-40) and feature L12 represents a diffusion region including feature 610 which is a part of different layer (col. 7, ll.34-37);

claim 62: the defined property specifies a plurality of alternative relationships between the first edge and the second edge within the multi-edge structure with multiple-relational variables (col. 4, ll.1-4);

claim 63: the second edge being contiguous with and substantially perpendicular to the first edge, and wherein the first shape further comprises a third edge, the third edge being contiguous with and substantially perpendicular to the second edge, the third edge being substantially parallel to and side-by-side with the first edge as shown on the Fig. 4C wherein the first shape comprises a first edge, a second edge, the second edge being contiguous with and substantially perpendicular to the first edge, a third edge, the third edge being contiguous with and substantially perpendicular to the second edge and the third edge and the first edge are substantially adjacent (side-by-side);

claim 64: the second edge being contiguous with and substantially perpendicular to the first edge as shown on the Fig. 6d, wherein the entire collection of edges 661-673 as a single shape (col. 7, ll.65-67; col. 8, ll.1-2) and the first edge 661 is contiguous with and substantially perpendicular to the second edge 662; wherein the first shape further comprises: a third edge 663, the third edge being contiguous with and substantially perpendicular to the second edge 662, wherein the third edge 663 is not substantially side-by-side with the first edge 661; a fourth edge 664, the fourth edge 664 being contiguous with and substantially perpendicular to the third edge 663, wherein the fourth edge is not substantially side-by-side with the second edge 662; a fifth edge 665, the fifth edge 665 being contiguous with and substantially perpendicular to the fourth edge 664, wherein the fifth edge is substantially parallel to and side-by-side with the third

edge 663; a sixth edge 666, the sixth edge 666 being contiguous with and substantially perpendicular to the fifth edge 665, wherein the sixth edge is not substantially side-by-side with the fourth edge 664; and a seventh edge 667, the seventh edge being contiguous with and substantially perpendicular to the sixth edge, the seventh edge being substantially parallel to and side-by-side with the first edge;

With respect to claim 65 Agrawal et al. teaches a method for correcting a plurality of layout imperfections in IC layout imperfections in an integrated circuit layout using the **shape-based approach** which enables accurate and efficient application of **layout modifications** (col. 14, ll.16-19; col. 5, ll.51-52; col. 8, ll.45-48), the method comprising: defining a plurality of shapes, each of the plurality of shapes comprising at least a first edge and a second edge related according to at least one of a plurality of defined properties, each of the plurality of shapes matching at least one of the plurality of layout imperfections within a catalog of defined shapes (abstract) comprising a first edge and a second edge coupled (related) in accordance with a first plurality of properties associated with the first shape (col. 14, ll.20-23); defining a plurality of actions to correct the plurality of layout imperfections, each of the plurality of actions being associated with at least one of the plurality of shapes within plurality of shapes defined in the catalog of shapes and layout **processing actions** associated with the various shapes (abstract); applying the plurality of actions to the IC layout responsive to the at least one of the plurality of shapes associated with each of the plurality of actions matching elements within the OC layout within applying layout processing actions associated with

the various shapes, wherein each layout processing action applies a specified layout **modification** to its associated shape (abstract).

With respect to claims 66-71 Agrawal et al. teaches:

claim 66: the plurality of actions having a specified sequence, wherein any element within the IC layout to which one of the plurality of actions is applied is excluded from further applications of the plurality of actions within the process of applying the appropriate layout processing actions to match portions of the IC layout as a sequential mode (abstract) using the conception depicted on the Fig. 10b wherein data controller 1032 performs sequential supply operation along with shape scanner 1034 and action manager and having the feature to be modified only once 1036 (col. 13, ll.2-8; col. 4, ll.19-22; col. 11, ll.31-36);

claim 67: the specified sequence being determined according to a predefined ranking of layout imperfection criticality within the scanning operation is performed in the order predefined by complexity of the shape and may be set by user desire (col. 4, ll.22-27);

claim 68: the IC layout comprising a plurality of polygons, each of the plurality of polygons comprising a plurality of elements having a portion if IC comprising plurality of layout features (polygons) (col. 14, ll.16-19), wherein applying the plurality of actions to the IC layout comprises: applying the plurality of actions to the plurality of elements included in a first polygon in the plurality of polygons in a specified sequence using the conception depicted on the Fig. 10b wherein data controller 1032 performs sequential supply operation along with shape scanner 1034 and action manager and having the feature to be modified only once 1036 (col. 13, ll.2-8; col. 4, ll.19-22); and restarting the

specified sequence when one of the plurality of actions is applied to one of the elements of the IC layout included in the first polygon using data controller 1032 for supplying a new primitive to shape scanner 1034 using loop B as shown on the Fig. 10b, where the loop B continues until all the elements in data controller 1032 have been processed (col. 13, ll.6-9);

claim 69: applying a first action to the IC layout responsive to the at least one the plurality of shapes associated with the first action matching elements in the IC layout (col. 14, ll.31); and applying a second action to the IC layout responsive to the at least one of the plurality of shapes associated with the second action matching elements in the IC layout (col. 14, ll.41-42);

claim 70: applying each of the plurality of actions to a first polygon in the plurality of polygons responsive to the at least one of the plurality of shapes associated with each of the plurality of actions matching elements in the first polygon using data controller 1032 for supplying a new primitive to shape scanner 1034 using loop B as shown on the Fig. 10b, where the loop B continues until all the elements in data controller 1032 have been processed (col. 13, ll.6-9); and applying each of the plurality of actions to a second polygon in the plurality of polygons responsive to the at least one of the plurality of shapes associated with the plurality of actions matching elements in the second polygon (primitives) within the loop B shown on the Fig. 10b (col. 13, ll.6-9);

claim 71: initializing a lookup table, the lookup table incorporating the plurality of actions within the bias table for collecting the layout processing actions (abstract) wherein the bias table is structured as lookup table (col. 2, ll.37-38; col. 8, ll.65-67; col. 9, ll.1-4).

With respect to claims 72 and 79 Agrawal et al. teaches a system for performing layout beautification on an integrated circuit layout data file within a shape-based OPC system 1000 shown on the Fig. 10a including input data file Dfin describing a particular IC layout (col. 12, ll.17-18; ll.21-22), the system comprising: an input data manager for loading the IC layout data file into the system using input data manager 1010 shown on the Fig. 10a (col. 12, l.19); a layout beautification engine for applying a plurality of corrective actions to the IC layout data file responsive to at least one of a plurality of shapes associated with each of the plurality of corrective actions matching elements in the IC layout data file, wherein each of the plurality of shapes comprises at least a first edge and a second edge related according to at least one of a plurality of defined properties within the OPC engine 1030 for performing shape matching and action application to the set of plurality of geometries (col. 12, ll.49-50), wherein OPC engine 1030 comprises a data controller 1032, a shape scanner 1034 and an action manager 1036 as shown on the Fig. 10b (col. 12, ll.51-60); and output data manager for generating an output data file within output data manager 1040 shown on the Fig. 10a (col. 12, ll.20-21).

With respect to claims 73-78 and 80-84 Agrawal et al. teaches:

claims 73 and 80: the IC layout data file comprises a fractured data file within a definition of a fracturing operation which is comprised in the first action being to match the first shape which is stored in the catalog of shapes (col. 18, ll.56-59), which is included into a input data file Dfin, and wherein loading the IC layout data file into the system comprises reassembling a plurality of layout primitives into a plurality of

polygons (col. 8, ll.42-44; col. 12, l.57) and wherein input data manager 1010 divides data file Dfin into its various layers and discrete sets of geometries within each layer (col. 12, ll.30-32);

claims 74 and 81: the IC layout data file having a first data file format, wherein loading the IC layout data file into the system comprises converting the first data file format into a second data file format, the layout beautification engine being configured to operate on the second data file format within the ability of the shape-based OPC system 1000 shown on the Fig. 10a to operate with any format data file Dfin, such as GDS, DXF, GIF etc. which is able to define the geometry of a integrated circuit layout (col. 12, ll.23-27) and ability of the data manager 1010 to convert input data file Dfin to a form that is operated by OPC system (col. 12, ll.28-29);

claims 75 and 82: generating the output data file comprises converting the second data file format into a third data file format within the output data manager 1040 shown on the Fig. 10a, which is able to convert the output data file into any format by the user desire (col. 13, ll.33-38; col. 16, ll.63-64);

claims 76 and 83: the layout beautification engine comprises a lookup table incorporating the plurality of corrective actions within the table 4 showing the actions defined by shape based OPC system for particular shapes (col. 9, ll.52-54);

claims 77 and 84: network connection to a remote storage location, wherein the remote storage location across at least one of the IC layout data file and the plurality of corrective actions as shown on the Fig. 11 wherein GDS database 1160 (standard

layout database) and an action/shape database 1160 are stored remotely via network storage location 1190 (col. 13, ll.51-54);

claim 78: the plurality of corrective actions are incorporated in a lookup table via bias tables (col. 13, ll.55-57).

With respect to claim 85 Agrawal et al. teaches a software program for performing layout beautification on a plurality of polygons in an integrated circuit (IC) layout, each of the plurality of polygons comprising a plurality of features, the software program (col. 19, ll.25-26; col. 20, ll.1-2) comprising: a first set of instructions for comparing a first shape to the plurality of features in each of the plurality of polygons to identify a first set of matching layout features, the first shape comprising at least a first edge and a second edge related according to a first property within the software wherein any programming code having plurality of sets of code has an ability of any sequence of having the instructions in the whole code (col. 20, ll.3-7; ll.20-23); a second set of instructions for performing a first layout beautificati6n action on each of the first set of matching layout features within the code processing a first action (first layout beautification action) within the software wherein any programming code having plurality of sets of code has an ability of any sequence of having the instructions in the whole code (col. 20, ll.24-25).

With respect to claims 86-88 Agrawal et al. teaches:

claim 86: the first layout beautification action comprises modifying each of the first set matching features by a fixed amount as shown on the Fig. 9b wherein a shape S_2 and a modified feature F_2 that could result from application of an action B (beatification

process) associated with shape S_2, wherein action narrows and lengthens finger structures matching shape S_2 by a particular amount (col. 10, ll.64-67);

claim 87: each of the first set of matching features comprises a different characteristics (properties), and wherein the first layout beautification action comprises performing a modification on each of the first set of matching features, the modification being based on the different characteristic of each of the first set of matching features within plurality of shapes wherein each shape having set of properties (characteristics) and layout processing actions are based on the properties (col. 3, ll.24-26; col. 6, ll.14-18);

claim 88: the first layout beautification action comprises replacing each of the first set of matching features with a second shape within the catalog of shapes specifying actions as functions of the property variables of the shapes (col. 8, ll.37-39; col. 10, ll.34-36).

With respect to claims 89 and 90 Agrawal et al. teaches an apparatus for reducing output data size in an input layout by beautifying the input layout by the system shown on the Fig. 11 including forming a grouping substantially similar in size and configuration to feature as shown on the Fig. 3a (col. 5, ll.59-61), the apparatus comprising: means for identifying a shape pattern in the input layout, wherein the shape pattern comprises at least a first edge and a second edge related according to at least one of a plurality of defined properties (col. 14, ll.20-24); and means for replacing the identified shape pattern with an alternative configuration, the alternative configuration reducing data volume by using a "wildcard" that allows the shape to identify a range of actual layout features as shown on the Fig. 7d (col. 8, ll.18-21); the alternative configuration provides one of and absolute correction, an adaptive correction, and a

replacement correction by using model-based actions, when fixed value adjustment is made, rule-based actions, when adjustment depends on actual characteristics, and shape-based actions, when action with replacement shapes respectively (abstract).

With respect to claim 91 Agrawal et al. teaches a method of providing corrective actions to a layout based on shape analysis using the shape-based approach which enables accurate and efficient application of layout modifications (col. 14, ll.16-19; col. 5, ll.51-52; col. 8, ll.45-48), the method comprising: identifying shape patterns on the layout, wherein each shape pattern comprises at least a first edge and a second edge related according to at least one of a plurality of defined properties (col. 14., ll.20-23); modifying the layout according to corrective actions associated with the identified shape patterns, thereby removing at least one layout imperfection, wherein the corrective actions using the shape-based system for layout modification (col. 8, ll.45-48) include at least one of: performing a first operation using a fixed value associated with an existing layout parameter of an identified shape pattern as applying rule-based OPC (col. 4, l.49); performing a second operation that is a function of an existing layout parameter of an identified shape pattern as a model-based OPC actions (col. 4, l.50); performing a third operation that replaces an identified shape pattern as a filler-shapes (col. 4, ll.45-48).

With respect to claims 92-95 Agrawal et al. teaches:

claim 92: performing the first operation includes matching a dimensional specification of a design rule and the existing layout parameter as layout processing actions associated with the shapes can be rule-based (col. 3, ll.63-62);

claim 93: performing the first operation includes fixed biasing as shown in the Table 1 containing sample values for rules that would be applied to the edge (col. 2, ll.49-60);

claim 94: performing the second operation includes providing a corrective action proportional to the existing layout parameter as layout processing actions associated with the shapes as model-based as shown in the Table 4 (col.45-48);

claim 95: performing the second operation includes at least one proportional biasing and negative biasing as shown in the Table 4 wherein two actions applied to the same shape 420 such as rule-based and model-based actions (col. 9, ll.48-55).

With respect to claim 96 Agrawal et al. teaches a shape-based beautification method in a layout using the shape-based approach which enables accurate and efficient application of layout modifications (col. 14, ll.16-19; col. 5, ll.51-52; col. 8, ll.45-48), the method comprising: identifying a shape pattern on the layout (col. 14., ll.20-23); and applying at least one of an absolute correction using a fixed value associated with an existing layout parameter of an identified shape pattern as applying rule-based OPC (col. 4, l.49), an adaptive correction as a model-based OPC actions (col. 4, l.50), and a replacement correction to the identified shape pattern as a filler-shapes (col. 4, ll.45-48), thereby removing at least one layout imperfection and reducing fracturing data volume in the layout wherein the corrective actions using the shape-based system for layout modification (col. 8, ll.45-48) and dividing input data Dfin into its various layers and discrete sets of geometries within each layer (col. 12, ll.31-37).

With respect to claims 97-99 Agrawal et al. teaches:

claim 97: the absolute correction includes matching a dimensional specification of a design rule and an existing layout parameter of the identified shape pattern as layout processing actions associated with the shapes can be rule-based (col. 3, ll.63-62);

claim 98: the adaptive correction includes providing a corrective action proportional to the existing layout parameter as a model-based OPC actions (col. 4, l.50);

claim 99: the replacement correction replaces the identified shape pattern with a simplified shape pattern as a filler-shapes (col. 4, ll.45-48).

Remarks

In response to the Applicant's arguments that Agrawal et al. does not teach beautification or a layout imperfection Examiner states that Agrawal et al. discloses the same shape-based system as instant Application and may be used in any situation requiring improved identification of layout features (col. 8, ll.45-48), which is also demonstrated by Figures, for example Fig. 9b, where shape S_2 is imperfection and feature F_2 is processed beautification operation of action B according the definition of the instant Specification. Therefor Agrawal et al. reads into the instant claims using the same computer system (Fig. 11), programming code and conception of using the **shape-based approach**, which enables **accurate** and efficient application of **layout modifications** (col. 5, ll.51-52).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen Rossoshek whose telephone number is 571-272-1905. The examiner can normally be reached on 7:00-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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